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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/774,682	02/09/2004	Thomas Rueckes	112020.129 US2 (Nan-6)	9428
23483	7590	04/19/2005	EXAMINER	
WILMER CUTLER PICKERING HALE AND DORR LLP			COLEMAN, WILLIAM D	
60 STATE STREET			ART UNIT	
BOSTON, MA 02109			PAPER NUMBER	

2823

DATE MAILED: 04/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/774,682

Applicant(s)

RUECKES ET AL.

Examiner

W. David Coleman

Art Unit

2823

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 09 February 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-15 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-15 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>02/04</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 2, 4, 5, 6, 7, 9, 10, 11, 12, 13, 14 and 15 are rejected under 35 U.S.C. 102(b) as being anticipated by Rueckes et al., “Carbon Nanotube-Based Nonvolatile Random Access Memory for Molecular Computing”, SCIENCE Magazine, July 7, 2000, vol. 289, pp 94-97. Rueckes discloses a semiconductor device as claimed. See FIGS. 1-4, where Rueckes teaches the claimed limitations.

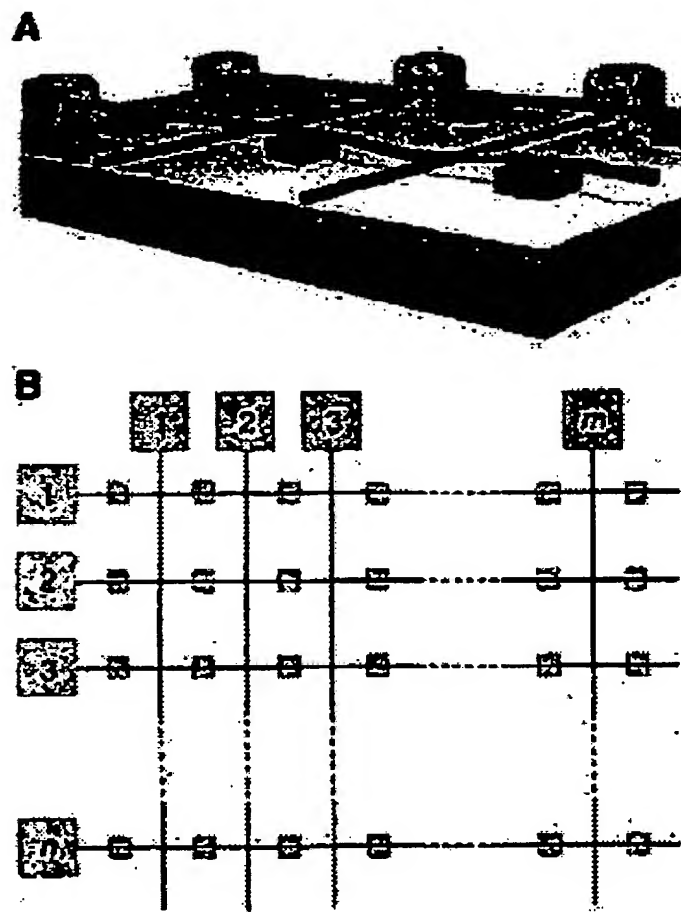


Fig. 1. Suspended nanotube device architecture. (A) Three-dimensional view of a suspended cross-bar array showing four junctions with two elements in the ON (contact) state and two elements in the OFF (separated) state. The substrate consists of a conducting layer [e.g., highly doped silicon (dark gray)] that terminates in a thin dielectric layer [e.g., SiO_2 (light gray)]. The lower nanotubes are supported directly on the dielectric film, whereas the upper nanotubes are suspended by periodic inorganic or organic supports (gray blocks). Each nanotube is contacted by a metal electrode (yellow blocks). (B) Top view of an n by m device array. The nanotubes in this view are represented by black crossing lines, and the support blocks for the suspended SWNTs are indicated by light gray squares. The electrodes used to address the nanotubes are indicated by yellow squares.

Art Unit: 2823

3. Pertaining to claim 1, Rueckes teaches an assembly including a substrate and a conductive trace disposed on the substrate, wherein the trace includes nanotube segments that contact other nanotube segments to define a plurality of conductive pathways along the trace.

4. Pertaining to claim 2, Rueckes teaches the assembly of claim 1 wherein the nanotube segments include single walled carbon nanotubes.

5. Pertaining to claim 4, Rueckes teaches the assembly of claim 1 wherein the nanotube segments have different lengths (see the explanation of figure 2D on page 95 where Rueckes discloses various minimum bistable device sizes).

6. Pertaining to claim 5, Rueckes teaches the assembly of claim 1 wherein the nanotube segments include segments having a length shorter than the length of the article (see the explanation above in the rejection of claim 4).

7. Pertaining to claim 6, Rueckes teaches an assembly including a substrate and a conductive trace disposed on the substrate, wherein the trace includes an electrical network of nanotubes in contact with other nanotubes to define a plurality of conductive pathways along the trace.

8. Pertaining to claim 7, Rueckes teaches the assembly of claim 6 wherein the nanotubes include single walled carbon nanotubes.

Art Unit: 2823

9. Pertaining to claim 9, Rueckes teaches the assembly of claim 6 wherein the nanotubes have different lengths.

10. Pertaining to claim 10, Rueckes teaches the assembly of claim 6 wherein the nanotubes include nanotubes having a length shorter than the length of the trace.

11. Pertaining to claim 11, Rueckes teaches an assembly including a substrate and a conductive trace of predefined shape, the conductive trace being over the substrate, the conductive trace including a plurality of nanotubes in electrical contact to form a plurality of conductive paths along the extent of the trace.

12. Pertaining to claim 12, Rueckes teaches an assembly including a substrate, at least one metal electrode, and a conductive trace of predefined shape, the conductive trace being over the substrate, the conductive trace including a plurality of nanotubes in electrical contact to form a plurality of conductive paths along the extent of the trace, and the metal electrode being over at least a portion of the conductive trace, the metal electrode being formed by a metalization step.

13. Pertaining to claim 13, Rueckes teaches a wafer substrate structure having a non-woven fabric of nanotubes covering a major surface of the wafer substrate and wherein the nanotubes of the fabric are arranged in accordance with inherent self-assembly traits of the nanotubes (see FIG. 1B).

Art Unit: 2823

14. Pertaining to claim 14, Rueckes teaches a wafer substrate structure having a non-woven fabric of nanotubes covering a major surface of the wafer substrate and wherein the fabric is substantially a monolayer of nanotubes.

15. Pertaining to claim 15, Rueckes teaches a wafer substrate structure having a non-woven fabric of nanotubes covering a major surface of the wafer substrate and wherein the fabric has a controlled density of nanotubes.

Claim Rejections - 35 USC § 103

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

17. Claims 3 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rueckes et al., “Carbon Nanotube-Based Nonvolatile Random Access Memory for Molecular Computing”, SCIENCE Magazine, July 7, 2000, vol. 289, pp 94-97, as applied to claims 1, 2, 4-7 and 9-15 above, and further in view of Lieber et al., U.S. Patent 6,743,408 B2.

18. Rueckes fails to teach the assembly of claims 1 and 6 wherein the nanotubes include multi-walled carbon nanotubes. Lieber teaches wherein the nanotubes include multi-walled carbon nanotubes. In view of Lieber, it would have been obvious to one of ordinary skill in the art to incorporate the multi-walled carbon nanotubes of Lieber into the Rueckes semiconductor device because they may be used as memory storage devices (column 7, lines 27-28).

Conclusion

19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to W. David Coleman whose telephone number is 571-272-1856.

The examiner can normally be reached on Monday-Friday 9:00 AM - 5:30 PM.

20. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

21. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



W. David Coleman
Primary Examiner
Art Unit 2823

WDC